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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,525	09/29/2003	John Bruno	00100.03.0034	6091

29153 7590 01/20/2006

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EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 01/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,525	BRUNO ET AL.	
	Examiner	Art Unit	
	James Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2003 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☒ Claim(s) *18 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2003 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *29 September 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responding to application 10/675525 originally received September 29, 2003. The amended claims received February 26, 2004 were used for this Office Action.

Claim Objections

Claims 18 and 31 are objected to because of the following informalities:

- In re claim 18, line 1 reads: "The method of claim 18 further..." Examiner asserts that applicant intended to refer to claim 17 instead of 18. Please change to read: "The method of claim 17 further..."
- In re claim 31, line 1 reads: "The method of claim 28 wherein..." Examiner asserts that applicant intended to refer to claim 30 instead of 28. Please change to read: "The method of claim 30 wherein..."

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 20 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Borkar et al. (U.S. Patent No. 6,484,265 B2) (hereinafter referred to as Borkar).

As to **claim 20**, Borkar discloses a method for generating a clock signal having an operating frequency set to a first frequency corresponding to a first junction temperature, the method comprising:

- detecting a junction temperature (via temperature sensor 136) corresponding to at least a portion of a circuit on a die (column 4, lines 13-20); and
- increasing the operating frequency of the clock signal above the first frequency to at least one of a second frequency corresponding to a second junction temperature and a third frequency corresponding to a third junction temperature, when the detected junction temperature is less than at least one of: the second junction temperature and the third junction temperature, such that second junction temperature and the third junction temperature is less than the first junction temperature (Borkar discloses increasing the frequency of a processor [114] via control circuit [118] to either a first frequency if TPROC is less than TLOW or to a second frequency if TPROC is between TLOW and THIGH; column 4, lines 21-46).

As to **claim 25**, Borkar discloses a method further comprising reducing at least one of: the frequency of the clock signal, and a supply voltage to at least the portion of the circuit on the die, if the detected junction temperature is above a junction temperature threshold (Borkar discloses a system change that can be made to the processor [114] via control circuit [118] to either the supply voltage, the frequency and/or bias voltage; column 4, lines 21-46).

Claims 26-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Helms et al. (U.S. Patent No. 6,889,332 B2) (hereinafter referred to as Helms).

As to **claim 26**, Helms discloses a method for generating a clock signal having an operating frequency comprising:

- detecting a junction temperature corresponding to at least a portion of a circuit on a die (column 3, lines 9-27);
- decreasing the operating frequency of the clock signal from a first frequency to a second frequency and selecting a new upper junction temperature threshold ("trip points") and a new lower junction temperature threshold ("trip points") that is higher than an upper junction temperature threshold if the detected junction temperature is above the upper junction temperature threshold (Helms discloses dynamically altering the thresholds ["trip points"] that are necessary to change the frequency of a processor [301] dependent on present and past operating criteria; column 2, lines 13-54 and column 3, lines 9-33 and column 6, lines 41-65 and column 7, line 19 thru column 8, line 55); and

- increasing the operating frequency of the clock signal from the first frequency to a third frequency and selecting the new higher upper junction temperature threshold and the new lower junction temperature threshold ("trip points") that is lower than a lower junction temperature threshold ("trip points") if the detected junction temperature is below the lower junction temperature threshold (Helms discloses dynamically altering the thresholds ["trip points"] that are necessary to change the frequency of a processor [301] dependent on present and past operating criteria; column 2, lines 13-54 and column 3, lines 9-33 and column 6, lines 41-65 and column 7, line 19 thru column 8, line 55).

As to **claim 27**, Helms discloses a method further including producing an interrupt control signal if the detected junction temperature is at least one of: below the lower junction temperature threshold, and above the upper junction temperature threshold (column 8, lines 56-67).

As to **claim 28**, Helms discloses a method wherein increasing and decreasing the operating frequency of the clock signal occurs over a transition time period such that increasing and decreasing the operating frequency of the clock signal includes at least one intermediate frequency (Helms discloses altering the frequency with a duty cycle and period appropriate for the processor; column 6, lines 51-57).

As to **claim 29**, Helms discloses a method further comprising reducing at least one of: the frequency of the clock signal, and a supply voltage to at least the portion of the circuit on the die, if the detected junction temperature is above a maximum junction temperature threshold (column 3, lines 9-13 and column 7, lines 18-64).

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Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2-11, 16-19, 21, 23, 24, 30, 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borkar et al. (U.S. Patent No. 6,484,265 B2) (hereinafter referred to as Borkar) and Meynard (U.S. Patent Publication No. 2003/0229816 A1) (hereinafter referred to as Meynard).

As to **claim 1**, Borkar discloses a clock control system for generating a clock signal having an operating frequency set to a first frequency corresponding to a first junction temperature, comprising:

- a thermal sensor (136) operative to detect a junction temperature corresponding to at least a portion of a circuit on a die (column 4, lines 13-20); and

- a temperature dependent dynamic clock generator circuit (control circuit 118), operatively coupled to the thermal sensor (via 122), and operative to increase the operating frequency of the clock signal above the first frequency to at least one of: a second frequency corresponding to a second junction temperature and a third frequency corresponding to a third junction temperature, when the detected junction temperature is less than at least one of the second junction temperature and the third junction temperature, such that the second junction temperature and the third junction temperature is less than the first junction temperature (Borkar discloses increasing the frequency of a processor [114] via control circuit [118] to either a first frequency if TPROC is less than TLOW or to a second frequency if TPROC is between TLOW and THIGH; column 4, lines 21-46).

Borkar does not disclose a temperature dependent dynamic clock generator circuit that can overclock a processor.

Meynard teaches a clock controller system (230 and 270) for a system that can overclock the processor given the temperature of the system via sensor (280) (paragraphs 53-56).

It would have been obvious to one of ordinary skill of the art, having the teachings of Borkar and Meynard before him at the time the invention was made, to modify the control circuit disclosed by Borkar to use the overclocking capabilities as taught by Meynard.

One of ordinary skill in the art would be motivated to make use of overclocking via clock control circuit in view of the teachings of Meynard, as doing so would allow the activity of the system to determine saturation and stalls in the system (paragraphs 11-13).

As to **claim 2**, Borkar discloses a clock control system wherein the temperature dependent dynamic overclock generator circuit provides hysteresis based frequency control (column 4, lines 40-43) to increase the operating frequency of the clock signal above the first frequency to at least one of the second frequency and the third frequency if the detected junction temperature is below a lower junction temperature threshold, and the temperature dependent dynamic overclock generator circuit decreases the operating frequency of the clock signal below at least one of the second overclock frequency and the third overclock frequency to the first frequency if the detected junction temperature is above an upper junction temperature threshold wherein the upper junction temperature threshold is greater than the lower junction temperature threshold (Borkar discloses increasing the frequency of a processor [114] via control circuit [118] to either a first frequency if TPROC is less than TLOW or to a second frequency if TPROC is between TLOW and THIGH; column 4, lines 21-46).

As to **claim 3**, Meynard teaches a clock control system wherein the first junction temperature is a maximum rated junction temperature of at least the portion of the circuit on the die (Meynard teaches a clock generation system that allows the processor to be overclocked above the manufacture's suggestions and therefore giving the first junction temperature the ability to be the maximum rated temperature for the processor; paragraphs 4-6 and 28).

As to **claim 4**, Meynard teaches a clock control system wherein the temperature dependent dynamic overclock generator circuit dynamically varies the frequency of the clock signal between the first frequency and at least one of the second frequency and the third frequency over a transition time period (Meynard discloses a "transition period" necessary to change frequencies; paragraphs 37 and 40-46).

As to **claim 5**, Borkar discloses a clock control system wherein the temperature dependent dynamic overclock generator circuit reduces at least one of: the frequency of the clock signal and a supply voltage to at least the portion of the circuit on the die if the detected junction temperature is above a junction temperature threshold (column 3, line 59 thru column 4, line 46).

As to **claim 6**, Borkar discloses a clock control system for generating a clock signal having an operating frequency set to a first frequency corresponding to a first junction temperature, comprising:

- a thermal sensor (136) operative to detect a junction temperature corresponding to at least a portion of a circuit on a die (column 4, lines 13-20); and
- a temperature dependent dynamic clock generator circuit (control circuit 118), operatively coupled to the thermal sensor (via 122), and operative to increase the operating frequency when the detected junction temperature is below threshold temperature (column 4, lines 13-46).

Borkar does not disclose a temperature dependent dynamic clock generator circuit that can overclock a processor where the operating frequency is set above the nominal frequency of the processor.

Meynard teaches a clock controller system (230 and 270) for a system that can overclock (therefore above the nominal frequency) the processor given the temperature of the system via sensor (280) (paragraphs 29 and 53-56).

It would have been obvious to one of ordinary skill of the art, having the teachings of Borkar and Meynard before him at the time the invention was made, to modify the control circuit disclosed by Borkar to use the overclocking capabilities as taught by Meynard.

One of ordinary skill in the art would be motivated to make use of overclocking via clock control circuit in view of the teachings of Meynard, as doing so would allow the activity of the system to determine saturation and stalls in the system (paragraphs 11-13).

As to **claim 7**, Borkar discloses a clock control system wherein the temperature dependent dynamic clock generator circuit (118) further includes:

- a clock generator circuit (324) operative to produce the clock signal (column 13, line 57 thru column 14, line 2); and
- temperature dependent dynamic clock control logic (118), operatively coupled to the thermal sensor (via 240) and operative to receive the temperature signal (as indicated by arrow direction for bus 122 in figure 1); and operatively coupled to the clock generator circuit (via 190), and operative to provide (as indicated by

arrow direction for bus 190 in figure 9) dynamic overclock frequency control data to the clock generator circuit (324) in response to the received temperature signal to increase the operating frequency of the clock signal when the detected junction temperature is less than a threshold temperature (column 4, lines 13-46 and column 13, line 57 thru column 14, line 2).

Meynard provides the capability of overclocking the processor above the nominal frequency when the junction temperature is below the maximum junction temperature (as shown above in claim 6; paragraphs 29 and 53-56).

As to **claim 8**, Borkar discloses a clock control system wherein the temperature dependent dynamic clock control logic (118) is operative to provide hysteresis based frequency control (column 4, lines 40-43) to: increase the operating frequency of the clock signal if the detected junction temperature is below a lower junction temperature threshold, and to decrease the operating frequency of the clock signal if the detected junction temperature is above an upper junction temperature threshold wherein the upper junction temperature threshold is greater than the lower junction temperature threshold (Borkar discloses increasing or decreasing the frequency of a processor [114] via control circuit [118] to either a first frequency if TPROC is less than TLOW or to a second frequency if TPROC is between TLOW and THIGH and vice versa; column 4, lines 21-46).

Meynard provides the capability of overclocking the processor above the nominal frequency when the junction temperature is below the maximum junction temperature (paragraphs 29 and 53-56).

As to **claim 9**, Borkar discloses a clock control system wherein the temperature dependent dynamic clock control logic (118) is operative to cause the clock generator circuit (324) to increase the operating frequency of the clock signal such that the detected junction temperature does not exceed a threshold junction temperature (column 4, lines 13-46).

Meynard provides the capability of overclocking the processor above the nominal frequency such that the detected junction temperature does not exceed a threshold junction temperature (as shown above in claim 6; paragraphs 29 and 53-56).

As to **claim 10**, Meynard teaches a clock control system wherein the temperature dependent dynamic overclock control logic (from Meynard) is operative to vary the operating frequency of the clock signal over a transition time period ("transition period"; paragraphs 37 and 40-46).

As to **claim 11**, Borkar discloses a clock control system wherein the temperature dependent dynamic overclock control logic (118) is operative to reduce at least one of: the operating frequency of the clock signal and a supply voltage to at least the portion of the circuit

on the die if the detected junction temperature is above a junction temperature threshold (column 3, line 59 thru column 4, line 46).

As to **claim 17**, Borkar discloses a method for generating a clock signal having an operating frequency set corresponding to a threshold temperature, the method comprising:

- detecting a junction temperature (via sensor 136) corresponding to at least a portion of a circuit on a die (column 4, lines 13-20); and
- increasing the operating frequency of the clock signal when the detected junction temperature is below a threshold temperature (column 3, line 59 thru column 4, line 46).

Borkar does not disclose a method that can overclock a processor where the operating frequency is set above the nominal frequency of the processor if the junction temperature is below a maximum rated temperature.

Meynard teaches a clock controller system (230 and 270) for a system that can overclock (therefore above the nominal frequency) the processor given the temperature of the system via sensor (280) (paragraphs 29 and 53-56).

It would have been obvious to one of ordinary skill of the art, having the teachings of Borkar and Meynard before him at the time the invention was made, to modify the control circuit disclosed by Borkar to use the overclocking capabilities as taught by Meynard.

One of ordinary skill in the art would be motivated to make use of overclocking via clock control circuit in view of the teachings of Meynard, as doing so would allow the activity of the system to determine saturation and stalls in the system (paragraphs 11-13).

As to **claim 18**, Meynard teaches a method further including decreasing the operating frequency of the clock signal below the nominal operating frequency when the detected junction temperature is above the maximum rated junction temperature (Meynard teaches forcing the frequency back to a first in response to the processor temperature; paragraph 29).

As to **claim 19**, Borkar discloses a method further including providing hysteresis based frequency control (column 4, lines 40-43) by: decreasing the operating frequency of the clock signal if the detected junction temperature is above an upper junction temperature threshold, and increasing the operating frequency of the clock signal if the detected junction temperature is below a lower junction temperature threshold wherein the upper junction temperature threshold is greater than the lower junction temperature threshold (Borkar discloses increasing or decreasing the frequency of a processor [114] via control circuit [118] to either a first frequency if TPROC is less than TLOW or to a second frequency if TPROC is between TLOW and THIGH and vice versa; column 4, lines 21-46).

As to **claim 21**, Borkar discloses a method further including providing hysteresis based frequency control (column 4, lines 40-43) by: decreasing the operating frequency of the clock

signal if the detected junction temperature is above an upper junction temperature threshold, and increasing the operating frequency of the clock signal if the detected junction temperature is below a lower junction temperature threshold wherein the upper junction temperature threshold is greater than the lower junction temperature threshold (Borkar discloses increasing or decreasing the frequency of a processor [114] via control circuit [118] to either a first frequency if TPROC is less than TLOW or to a second frequency if TPROC is between TLOW and THIGH and vice versa; column 4, lines 21-46).

As to **claim 23**, Borkar discloses a method wherein the first junction temperature is measured on at least a portion of the die of the processor (column 4, lines 21-46).

Borkar does not disclose a method that can overclock a processor where the first junction temperature is a maximum rated junction temperature and the corresponding first frequency is a nominal operating frequency of the clock signal.

Meynard teaches a clock controller system (230 and 270) for a system that can overclock (therefore above the nominal frequency) the processor given the temperature of the system via sensor (280) (paragraphs 29 and 53-56).

It would have been obvious to one of ordinary skill of the art, having the teachings of Borkar and Meynard before him at the time the invention was made, to modify the control circuit disclosed by Borkar to use the overclocking capabilities as taught by Meynard.

One of ordinary skill in the art would be motivated to make use of overclocking via clock control circuit in view of the teachings of Meynard, as doing so would allow the activity of the system to determine saturation and stalls in the system (paragraphs 11-13).

As to **claim 24**, Borkar discloses method wherein the operating frequency is increased in response to a junction temperature crossing a threshold.

Borkar does not disclose a method that can overclock a processor where increasing the clock signal happens over a transition period such that the operating frequency is increasing, the clock signal includes at least one intermediate frequency.

Meynard teaches a clock controller system (230 and 270) for a system that can overclock (therefore above the nominal frequency) the processor given the temperature of the system via sensor (280) (paragraphs 29 and 53-56). The transition from one frequency to another is to be carried out in an appropriate amount of time (paragraphs 37 and 40-46) .

It would have been obvious to one of ordinary skill of the art, having the teachings of Borkar and Meynard before him at the time the invention was made, to modify the control circuit disclosed by Borkar to use the overclocking and transition capabilities as taught by Meynard.

One of ordinary skill in the art would be motivated to make use of overclocking via clock control circuit with appropriate transition times in view of the teachings of Meynard, as doing so would allow the activity of the system to determine saturation and stalls in the system (paragraphs 11-13).

As to **claim 30**, Borkar discloses a method for generating a clock signal having an operating frequency set corresponding to a threshold temperature, the method comprising:

- detecting a junction temperature (via sensor 136) corresponding to at least a portion of a circuit on a die (column 4, lines 13-20);
- increasing the operating frequency of the clock signal to a first frequency when the detected junction temperature is less than a first junction temperature associated with the first frequency (column 3, line 59 thru column 4, line 46); and
- increasing the operating frequency of the clock signal to a second frequency above the first frequency, when the detected junction temperature is less than a second junction temperature associated with the second frequency, such that the second junction temperature is less than the first junction temperature (column 3, line 59 thru column 4, line 46).

Borkar does not disclose a method that can overclock a processor where the operating frequency is set above the nominal frequency of the processor if the junction temperature is below a maximum rated temperature.

Meynard teaches a clock controller system (230 and 270) for a system that can overclock (therefore above the nominal frequency) the processor given the temperature of the system via sensor (280) (paragraphs 29 and 53-56).

It would have been obvious to one of ordinary skill of the art, having the teachings of Borkar and Meynard before him at the time the invention was made, to modify the control circuit disclosed by Borkar to use the overclocking capabilities as taught by Meynard.

One of ordinary skill in the art would be motivated to make use of overclocking via clock control circuit in view of the teachings of Meynard, as doing so would allow the activity of the system to determine saturation and stalls in the system (paragraphs 11-13).

As to **claim 32**, Borkar discloses a memory containing instructions executable by one or more processing devices (114) that causes the one or more processing devices to:

- detect a junction temperature corresponding to at least a portion of a circuit on a die (column 7, lines 50-67);
- increase an operating frequency of a clock signal associated with at least the portion of the circuit on the die when the detected junction temperature is below a threshold temperature (column 4, lines 21-46 and column 7, lines 50-67).

Borkar does not disclose a method that can overclock a processor where the operating frequency is set above the nominal frequency of the processor if the junction temperature is below a maximum rated temperature.

Meynard teaches a clock controller system (230 and 270) for a system that can overclock (therefore above the nominal frequency) the processor given the temperature of the system via sensor (280) (paragraphs 29 and 53-56).

It would have been obvious to one of ordinary skill of the art, having the teachings of Borkar and Meynard before him at the time the invention was made, to modify the control circuit disclosed by Borkar to use the overclocking capabilities as taught by Meynard.

One of ordinary skill in the art would be motivated to make use of overclocking via clock control circuit in view of the teachings of Meynard, as doing so would allow the activity of the system to determine saturation and stalls in the system (paragraphs 11-13).

As to **claim 33**, Borkar discloses a memory containing executable instructions that causes the one or more processing devices to:

- decrease the operating frequency of the clock signal if the detected junction temperature is above an upper junction temperature threshold (column 7, lines 50-67); and
- increase the operating frequency of the clock signal if the detected junction temperature is below a lower junction temperature threshold (column 7, lines 50-67).

Claims 12, 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahalingaiah et al. (U.S. Patent No. 5,490,059) (hereinafter referred to as Mahalingaiah) and Meynard (U.S. Patent Publication No. 2003/0229816 A1) (hereinafter referred to as Meynard).

As to **claim 12**, Mahalingaiah discloses a clock control system for generating a clock signal having an operating frequency set to a first operating frequency corresponding to a threshold temperature, comprising:

- a thermal sensor (temperature sensor 130) operative to produce a temperature signal corresponding to a junction temperature of at least a portion of a circuit on a die (column 3, lines 41-49);
- a thermal sensor control circuit (control unit 134), operatively coupled (via 132) to the thermal sensor (130), and operative to produce temperature data in response to the temperature signal (column 6, lines 13-35);
- a clock generator circuit (frequency synthesizer) operative to produce the clock signal (column 3, lines 33-40); and
- a dynamic overclock frequency control data generator (control unit 134), operatively coupled to the thermal sensor control circuit (incorporated within 134) and operative to receive the temperature data (from sensor 130), and operatively coupled to the clock generator circuit (via bus 122), and operative to provide dynamic overclock frequency control data to the clock generator circuit in response to the received temperature data to cause the clock generator circuit to increase the operating frequency of the clock signal when the detected junction temperature is less than a threshold temperature (column 3, lines 50 thru column 5, lines 42).

Mahalingaiah does not disclose a method that can overclock a processor where the operating frequency is set above the nominal frequency of the processor if the junction temperature is below a maximum rated temperature.

Meynard teaches a clock controller system (230 and 270) for a system that can overclock (therefore above the nominal frequency) the processor given the temperature of the system via sensor (280) (paragraphs 29 and 53-56).

It would have been obvious to one of ordinary skill of the art, having the teachings of Mahalingaiah and Meynard before him at the time the invention was made, to modify the control circuit disclosed by Mahalingaiah to use the overclocking capabilities as taught by Meynard.

One of ordinary skill in the art would be motivated to make use of overclocking via clock control circuit in view of the teachings of Meynard, as doing so would allow the activity of the system to determine saturation and stalls in the system (paragraphs 11-13).

As to **claim 13**, Mahalingaiah discloses a clock control system wherein the dynamic clock frequency control data generator (control unit 134) is operative to provide hysteresis (column 3, lines 6-15) based frequency control to increase the operating frequency of the clock signal if the detected junction temperature is below a lower junction temperature threshold, and the temperature dependent dynamic overclock generator circuit decreases the operating frequency of the clock signal if the detected junction temperature is above an upper junction temperature threshold wherein the upper junction temperature threshold is greater than the lower junction temperature threshold (column 3, lines 50 thru column 5, lines 42).

Meynard provides the capability of overclocking the processor above or below the nominal frequency such that the overclocking is dependent on the maximum rated temperature (paragraphs 29 and 53-56).

As to **claim 16**, Mahalingaiah discloses a clock control system wherein the dynamic overclock frequency control data generator (control unit 134) is operative to reduce the frequency of the clock signal to at least the portion of the circuit on the die if the first junction temperature is above a junction temperature threshold (column 3, lines 33-40).

Claims 22 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borkar et al. (U.S. Patent No. 6,484,265 B2) (hereinafter referred to as Borkar) and Meynard (U.S. Patent Publication No. 2003/0229816 A1) (hereinafter referred to as Meynard) as applied to claims 1, 6, 7, 12, 17, 18 and 30 above, and further in view of Helms et al. (U.S. Patent No. 6,889,332 B2) (hereinafter referred to as Helms).

As to **claim 22**, Borkar discloses a method including temperature dependent clock control circuit (118) where there may be hysteresis capabilities expressed but no details are revealed (column 4, lines 21-46).

Helms discloses a temperature dependent clock control circuit (307) that has the capabilities of altering thresholds to determine frequency changes of a processor (301) wherein the method is selecting a new upper junction temperature threshold and a new lower junction temperature threshold that is greater than the upper junction temperature threshold if the detected

junction temperature is above the upper junction temperature threshold, and selecting the new upper junction temperature threshold and the new lower junction temperature threshold that is lower than the lower junction temperature threshold if the detected junction temperature is below the lower junction temperature threshold (column 2, lines 13-54 and column 7, line 20 thru column 8, line 55).

It would have been obvious to one of ordinary skill of the art, having the teachings of Borkar, Meynard and Helms before him at the time the invention was made, to modify the method of generating a clock signal disclosed by Borkar and Meynard to use hysteresis threshold altering capabilities as taught by Helms.

One of ordinary skill in the art would be motivated to make use of hysteresis threshold altering capabilities in view of the teachings of Helms, as doing so would give the added benefit of power savings (column 4, lines 60-64).

As to **claim 31**, Borkar and Meynard do not teach a method wherein increasing the operating frequency of the clock signal occurs over a transition time period such that as the operating frequency is increasing, the clock signal includes at least one intermediate frequency.

Helms teaches a dynamic clock control circuit using hysteresis wherein the transition period for switching frequencies is at least one intermediate frequency (Helms teaches altering the frequency with a duty cycle and period appropriate for the processor; column 6, lines 51-57).

It would have been obvious to one of ordinary skill of the art, having the teachings of Borkar, Meynard and Helms before him at the time the invention was made, to modify the clock

generating method disclosed by Borkar and Meynard to use the frequency transition properties as taught by Helms.

One of ordinary skill in the art would be motivated to make use of frequency transition properties in view of the teachings of Helms, as doing so would give the added benefit of power savings (column 4, lines 60-64).

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahalingaiah et al. (U.S. Patent No. 5,490,059) (hereinafter referred to as Mahalingaiah) and Meynard (U.S. Patent Publication No. 2003/0229816 A1) (hereinafter referred to as Meynard) as applied to claim 12 above, and further in view of Borkar et al. (U.S. Patent No. 6,484,265 B2) (hereinafter referred to as Borkar) and Cheng et al. (U.S. Patent No. 6,963,992 B1) (hereinafter referred to as Cheng).

As to **claim 14**, Mahalingaiah and Meynard do not teach a clock control system wherein the thermal sensor control circuit further comprises an analog to digital converter, operatively coupled to the thermal sensor, and operative to produce the temperature data in response to the temperature signal.

Borkar teaches a dynamic frequency clock controller (118) wherein an analog-to-digital converter (258) is used including an integrator (252) to convert the temperature signal to a usable signal in the control circuitry (column 14, lines 38-50).

It would have been obvious to one of ordinary skill of the art, having the teachings of Mahalingaiah, Meynard and Borkar before him at the time the invention was made, to include

within the thermal control circuitry disclosed by Mahalingaiah and Meynard to use an A/D converter coupled to the thermal sensor as taught by Borkar.

One of ordinary skill in the art would be motivated to make use of an A/D converter within the thermal sensor control circuitry coupled to the thermal sensor in view of the teachings of Borkar, as doing so would give the added benefit of altering the voltage as well as the clock frequency (column 1, lines 59-65).

Mahalingaiah, Meynard and Borkar do not teach a thermal control circuitry that has an interrupt control circuit, operatively coupled to the analog to digital converter, and operative to provide an interrupt control signal to the dynamic overclock frequency control data generator in response to the temperature data.

Cheng teaches an overclocking recovery circuit (100) wherein the circuit is incorporated with an advanced programmable interrupt controller (column 3, lines 5-17).

It would have been obvious to one of ordinary skill of the art, having the teachings of Mahalingaiah, Meynard, Borkar and Cheng before him at the time the invention was made, to modify the thermal control circuit disclosed by Mahalingaiah, Meynard and Borkar to use an advanced programmable interrupt controller as taught by Cheng.

One of ordinary skill in the art would be motivated to make use of advanced programmable interrupt controller in view of the teachings of Cheng, as doing so would give the added benefit of resetting the processor if stalled while overclocking (column 1, line 60 thru column 2, line 5).

As to **claim 15**, Cheng teaches a clock control system wherein the interrupt control circuit is operative to produce the interrupt control signal in response to a comparison between the temperature data and the threshold temperature data, such that the dynamic overclock frequency control data generator is operative to produce the dynamic overclock frequency control data in response to the interrupt control signal (Cheng teaches resetting the processor if it becomes stalled while overclocking due to the heat created or other environmental variables involved; column 1, line 60 thru column 2, line 5 and).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

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January 17, 2006

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